Application No.: 10/734,296

REMARKS

Claims 1-32 stand rejected under 35 U.S.C. § 102 as being anticipated by Arimoto et al. '915 ("Arimoto"). This rejection is respectfully traversed for the following reasons.

A. Claim 1

i) a ground voltage is applied to the first bit line in a low level state

Claim 1 recites in pertinent part, "wherein ... a ground voltage is applied to the first bit line in a low level state." The Examiner relies on element BLL shown in Figure 4 of Arimoto as the claimed first bit line, and alleges that col. 3, lines 50-53 and col. 13, lines 4-13 discloses applying a ground voltage to the alleged first bit line BLL in a low level state.

However, col. 3, lines 50-53 of Arimoto is directed to the admitted prior art of Arimoto and has nothing to do with the disclosed embodiment of Figure 4 and the corresponding bit line BLL; and Arimoto does not suggest using the admitted prior art voltages in the disclosed device relied upon by the Examiner to read on the specified elements recited in claim 1.

In addition, col. 13, lines 4-13 of Arimoto is silent as to applying a ground voltage to the alleged first bit line **BLL**, but instead discloses that the "bit line isolation instructing signal **BLIL** is at a ground voltage level." In fact, col. 13, lines 4-13 of Arimoto appears to teach away from the claimed invention. Specifically, col. 13, lines 13-14 of Arimoto expressly discloses that "the bit line voltage at the L level ***can not be discharged to the ground voltage level***" (emphasis added).

In this regard, col. 8, lines 32-39 of Arimoto discloses the actual *non-ground* voltage applied to the bit lines in the low level state; namely, that "the bit line of the selected memory block receives a voltage of Vthp as an L level signal [where] Vthp is an absolute value of the threshold voltage of the P channel MOS transistor constituting the bit line isolation gate."

ii) the access transistor is a depletion type p-channel MISFET

Claim 1 further recites in pertinent part, "wherein the access transistor is a depletion type p-channel MISFET." The Examiner alleges that the access transistor MTR shown in Figure 1 is a depletion type by referencing col. 6, lines 54-56 and col. 7, lines 3-7 of Arimoto. However, the referenced portions of Arimoto appear to be completely silent as to whether the MTR is a depletion type. Specifically, col. 6, lines 54-56 merely refers to a logic transistor LTR having a threshold voltage Vth of a small absolute value, and is silent as to any access transistor let alone describe it as a depletion-type. Moreover, col. 7, lines 3-7 merely discloses that the memory transistor MTR is formed in the same manufacturing step as that of the logic transistor LTR. Indeed, according to such a description, Arimoto actually suggests that the memory transistor MTR (access transistor) is NOT a depletion type but rather an enhancement type as in the general logic transistor. In this regard, it should be noted that Arimoto expressly describes the memory cell transistor as having a threshold voltage set substantially at the same value as that of the logic transistor (*see* col. 11, lines 19-22).

B. Claim 12

i) the access transistor is a depletion type n-channel MISFET

Claim 12 recites in pertinent part, "wherein the access transistor is a depletion type n-channel MISFET." The Examiner alleges that the access transistor MTR shown in Figure 12 is a depletion type by referencing col. 6, lines 54-56 and col. 7, lines 3-7 of Arimoto. As a preliminary matter, based upon the written disclosure related to Figure 12, it would appear that the disclosed MTR of Figure 12 is a p-channel MOS transistor rather than an n-channel MOS transistor (*see* col. 15, line 66 - col. 16, line 8 of Arimoto). In any event, even assuming *arguendo* that the MTR is an n-channel MOS transistor, Arimoto fails to disclose whether the

transistor is a depletion type. As discussed above with respect to claim 1, the relied on portions at col. 6, lines 54-56 and col. 7, lines 3-7 of Arimoto appear to be completely silent as whether the MTR is a depletion type and instead actually suggest that the MTR is an enhancement type as in the general logic transistor.

ii. positive voltage is applied to a gate electrode of the access transistor

Claim 12 further recites in pertinent part, "wherein a positive power supply voltage is applied to the first bit line ..., wherein the positive voltage is applied to a gate electrode of the access transistor." However, the alleged positive voltage VCCS (sense power supply voltage; *see* col. 13, lines 4-13 of Arimoto) is NOT applied to the gate electrode of the alleged access transistor MTR *shown in Figure 12 as relied on by the Examiner to read on the claimed access transistor*. In contrast, as admitted by the Examiner and shown in Figure 12, VCCS + α (i.e., a higher voltage than alleged positive voltage VCCS) is applied to the gate electrode of the alleged access transistor MTR.

C. Claims 16 and 29

Claim 16 recites in pertinent part, "wherein the threshold voltage of the access transistor is set to be higher than that of the p-channel MISFET ..." (emphasis added) while claim 29 recites in pertinent part, "wherein the threshold voltage of the access transistor is set to be lower than the threshold voltage of the n-channel MISFET ..." (emphasis added). As a preliminary matter, it is noted that the Examiner relies on the same portion of Arimoto (i.e., col. 6, lines 54-59) as allegedly disclosing the aforementioned features of the present invention, evidencing that the Examiner apparently does not differentiate between the different features recited therein as indicated by the underlining above. Indeed, the Examiner appears to believe that both claims recite the threshold voltage of the access transistor being set to be higher than that of the p-

channel MISFET (recited in claim 16), without addressing the limitation recited in claim 29 in which the threshold voltage of the access transistor is set to be lower than the threshold voltage of the n-channel MISFET.

In any event, it is respectfully submitted that the relied on portions of Arimoto are completely silent as to the recited ***relative*** threshold voltages of the respective transistors. Specifically, col. 6, lines 54-59 merely describes the logic transistor having a low threshold, but does not suggest that the low threshold is either higher or lower than the alleged access transistor. Indeed, Arimoto does not compare the logic transistor's threshold voltage with the access transistor of the memory. In fact, as previously mentioned, it should be noted that Arimoto expressly describes the memory cell transistor (access transistor) as having a threshold voltage set substantially at the same value as that of the logic transistor (*see* col. 11, lines 19-22) so as to *teach away* from the claimed invention.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Arimoto does not anticipate claims 1, 12, 16 and 29, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1, 12, 16 and 29 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are

also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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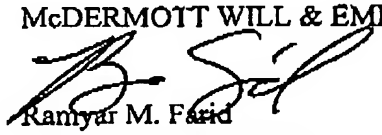

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